In the Claims:

Please amend claims 1, 3, 5, 10 and 13. Please cancel claim 6.

The claims are as follows:

1. (Currently Amended) An integrated circuit, comprising:

a multiplicity of identical macro-circuits, each ~~macro-circuit~~ macro-circuit of said multiplicity of identical macro-circuits being a logic circuit having the same function;

a fuse bank containing a multiplicity of fuses, ~~the~~ a state of said fuses storing test data indicating at least which macro-circuits failed a test; ~~and~~

a scan multiplexer and control circuit connected to scan-in I/O pads and scan-out I/O pads and connected to each of said identical macro-circuits, said scan multiplexer and control circuit including means for selectively connecting said scan-in I/O pads and scan-out I/O pads to and disconnecting said scan-in I/O pads and scan-out I/O pads from each of said macro-circuits of said multiplicity of identical macro-circuits during testing of said multiplicity of identical macro-circuits;

means for isolating each macro-circuit of said multiplicity of macro-circuits from any other logic circuits of said integrated circuit chip and means for connecting scan-in and scan-out pins dedicated to each macro-circuit of said multiplicity of macro-circuits to respective pads of said scan-in I/O pads and scan-out I/O pads;

means for permanently preventing utilization of those macro-circuits during operation of said integrated circuit that did not pass said test ~~failing macro-circuits~~ during operation of said integrated circuit, said means for permanently preventing responsive to said state of fuses in said fuse bank.

2. (Original) The integrated circuit of claim 1, further including means for isolating inputs and outputs of said macro-circuit during testing of said macro-circuits and during testing of additional circuits of said integrated circuit.

3. (Currently Amended) The integrated circuit of claim 1, further including:

~~isolation circuits adapted to,~~ means for isolating said macro-circuits during testing of said macro-circuits~~, isolate each macro-circuit~~ from additional circuits of said integrated circuit and from each other; and

~~couple a single~~ means for connecting one or more macro-circuits of said multiplicity of identical macro-circuits into a single scan chain, the output of said single scan chain observable at ~~an~~ a scan-out I/O pad of said scan-out I/O pads of said integrated circuit.

4. (Original) The integrated circuit of claim 1, wherein said macro-circuits include logic built-in test circuits.

5. (Currently Amended) The integrated circuit of claim 1, wherein said means for preventing includes (i) a shift register for reading out the state of said fuses and for passing the state of said fuses to ~~a control circuit, said control circuit adapted to disable~~ means for disabling failing macro-circuits directly in response to said state of said fuses ~~or adapted to disable~~ or (ii) means for disabling failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to in response to said state of said fuses.

6. (Canceled)

7. (Original) The integrated circuit of claim 1, wherein said macro-circuits are microprocessors and said means for preventing generates a busy signal for each macro-circuit that failed said test.

8. (Original) The integrated circuit of claim 1, wherein said fuse bank stores compressed data and further including means for decompressing said compressed data.

9. (Original) The integrated circuit of claim 1, wherein said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses.

10. (Currently Amended) A method of generating a partial good integrated circuit, the method comprising:

providing an integrated circuit having:

a multiplicity of identical macro-circuits arranged in one or more groups, each ~~macro circuit~~ macro-circuit of the same group being identical and having the same function[[,]]; ~~and~~

a fuse bank containing fuses[[, and]];

a scan multiplexer and control circuit connected to scan-in I/O pads and scan-out I/O pads and connected to each of said identical macro-circuits, said scan multiplexer and control circuit including means for selectively connecting said scan-in I/O pads and scan-out I/O pads to and disconnecting said scan-in I/O pads and scan-out I/O pads from each of said macro-circuits of said multiplicity of identical macro-circuits during testing of

said multiplicity of identical macro-circuits; and

means for isolating each macro-circuit of said multiplicity of macro-circuits from any other logic circuits of said integrated circuit chip and for means for connecting scan-in and scan-out pins dedicated to each macro-circuit of said multiplicity of macro-circuits to respective pads of said scan-in I/O pads and scan-out I/O pads;

isolating said macro-circuits from other circuits of said integrated circuit by connecting scan-in and scan-out pins dedicated to each macro-circuit of said multiplicity of macro-circuits to respective pads of said scan-in I/O pads and scan-out I/O pads;

testing each macro-circuit prior to a fuse programming operation;

programming said fuses in said fuse bank in order to store data indicating at least which macro-circuits failed said testing step; and

for each macro-circuit of said multiplicity of macro-circuits that failed said testing step, permanently preventing utilization of the entire ~~each~~ failing macro-circuit during operation of said integrated circuit based on the data stored in said fuse bank and configuring said integrated circuit to utilize only macro-circuits that passed said testing.

11. (Original) The method of claim 10, wherein:

said integrated circuit further includes first scan chains coupling said other circuits, second scan chains coupled to said macro-circuits and isolation circuits coupled to third scan chains, said isolation circuits coupled between said other circuits and said macro-circuits; and

further including the steps of coupling said first, second and third scan chains into a first configuration to achieve isolation of said other circuits from said macro-circuits and coupling said first, second and third scan chains into a second configuration to achieve isolation of said

macro-circuits from each other and from said other circuits.

12. (Original) The method of claim 10, wherein said testing includes applying sequentially one or more test patterns to each macro-circuit in each group macro-circuits and determining failing macro-circuits one group at a time.

13. (Currently Amended) The method of claim 10, further including keeping a count of failing macro-circuits during testing and terminating testing when the number of failing macro-circuits exceeds a predetermined ~~number~~ limit.

14. (Original) The method of claim 10, further including:

writing data indicating at least which macro-circuits failed to a fuse blow file in a tester performing said testing; and

wherein said programming is performed based on data in said fuse blow file.

15. (Original) The method of claim 10, further including:

performing a post fuse blow test, said post fuse blow test including in the order recited:

masking each failing macro-circuit based on the data in said fuse bank;

applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time; and

terminating post fuse blow test upon any macro-circuit failing.

16. (Original) The method of claim 15, further including in the order recited:

after performing said post fuse test, packaging said integrated circuit into a module; and

performing a module test, said module test including in the order recited:

masking each failing macro-circuit based on the data in said fuse bank;

applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time; and

terminating module test upon any macro-circuit failing.

17. (Original) The method of claim 10, wherein said macro-circuits are microprocessors.

18. (Original) The method of claim 10, wherein the step of preventing includes generating a busy signal for each macro-circuit that failed said test.

19. (Original) The method of claim 10, wherein the step of preventing includes disabling failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to.

20. (Original) The method of claim 10, wherein said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses.